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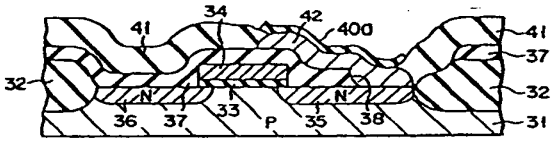
(54) Semiconductor read only memory device and method of manufacturing the same.

(57) A semiconductor read only memory device is disclosed, which comprises a plurality of memory cells each including drain and source regions (35, 36) separately formed on a semiconductor substrate (31) of p-conductivity type and a gate electrode (34) insulatively disposed over the semiconductor substrate and extending between the drain and source regions (35, 36). A poly-silicon layer containing an impurity of the p-conductivity type is formed such that it is contiguous to each drain region. A silicon nitride mask (40a) having electric insulation property and anti-oxidation property is formed selectively on the poly-silicon layer. The poly-silicon layer is oxidized selectively except for portions contiguous to the drain regions in the presence of the silicon nitride masks (40a). An aluminum layer (43) is selectively made in contact with the poly-silicon layer (42) depending on the presence or absence of the silicon nitride layer.



EP 0 186 855 A2

Semiconductor read only memory device and method of manufacturing the same

This invention relates to a semiconductor read only memory device and a method of manufacturing the same.

In the manufacture of a semiconductor read only memory (ROM), usually data is written in the ROM using a mask during the manufacture. Such a ROM is called mask program ROM. Data is written in the mask program ROM by using one of three, extensively employed data storage systems, i.e., a contact system, in which electrodes are selectively made in contact with memory cells, a SDG system, in which data is written depending on the presence or absence of transistor, and a system, in which the transistor threshold voltage is varied according to write data.

Meanwhile, ROMs are classified with respect to the circuit construction into those of a NOR type and those of a NAND-NOR type. The former ROMs are suited for high speed operation, and the latter for low speed operation.

With respect to the drive system, ROMs are classified into synchronizing ROMs and unsynchronizing ROMs.

The NOR-type ROM, suited for high speed operation, features readiness of circuit design and readiness and reliability of data writing. Further, the contact system is adopted for data writing, because a data writing step is in the latter half of the entire process of manufacture of the ROM.

In a ROM adopting the contact system, e.g., one disclosed in U.S. patent specification 603,698, where a wiring layer contiguous to the drain region of a MOS transistor is formed on a semiconductor substrate, a gate electrode is formed on the substrate before an insulation layer is formed on the substrate surface inclusive of the gate electrode. The insulation layer is formed with a contact hole for the drain region by photo-etching. A conductive layer is then formed on the insulation layer inclusive of the portion of the drain region exposed by the contact hole. The contact layer is patterned by photo-etching using a mask, whereby a contact electrode is formed in the drain region.

An insulation layer is formed on the entire surface of the semiconductor structure thus obtained. The insulation layer is selectively removed according to write data by photo-engraving process using a mask. A contact electrode contiguous to each intended drain region is thus exposed. Subsequently, aluminum wiring is connected to each exposed contact electrode to complete a ROM where data lines are formed.

In the above ROM, however, the processes of forming the contact electrode contiguous to each drain region and aluminum wiring require mask registration. The mask registration requires a certain margin. Therefore, when the number of mask registration processes is increased, it becomes impossible to realize a high density ROM.

The present invention seeks to provide a read only memory device, with permits memory cell size reduction and integration density increase without greatly changing the manufacturing process.

According to the invention, an insulating layer formed on a semiconductor substrate, on which MOS transistors constituting respective memory cells are formed, is selectively etched to form contact holes on drain regions. A poly-silicon layer is then formed on the insulation layer. At this time, the poly-silicon layer

is made in contact with the drain regions via the contact holes. A silicon nitride layer is then formed on the poly-silicon layer. The silicon nitride layer is selectively removed according to write data. The poly-silicon layer is selectively oxidized with the patterned silicon layer used as a mask, whereby electrodes in contact with the drain regions are formed.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Figs. 1A to 1E are views showing semiconductor structures in a process of manufacture of an embodiment of the semiconductor read only memory device according to the invention;

Fig. 2 is a plan view showing the same semiconductor read only memory device;

Fig. 3 is a sectional view of the semiconductor read only memory device;

Fig. 4 is a sectional view of the semiconductor read only memory device at a further embodiment;

Fig. 5 is a plan view showing the memory device shown in Fig. 4;

Fig. 6 is a sectional view showing a still further embodiment of the semiconductor read only memory device;

Figs. 7A and 7B show semiconductor structures in processes of manufacture of the semiconductor ROM shown in Fig. 6; and

Fig. 8 is a sectional view of the semiconductor read only memory device of a still further embodiment.

Figs. 1A to 1E illustrate a process of manufacturing a semiconductor read only device. As shown in Fig. 1A, p-type silicon substrate 31 is selectively oxidized to form field oxide layer 32 on it. Gate oxide layer 33 is then formed selectively on substrate 31. Then, on gate oxide layer 33 is formed gate electrode 34 made of a poly-silicon layer containing phosphorus. Gate electrode 34 is formed by a chemical vapor deposition

process (CVD) or a photo-engraving process. The poly-silicon layer may be doped with phosphorus after the formation of gate oxide layer 33 if phosphorus is not initially contained.

An n-type impurity, arsenic ions for instance, is then implanted into substrate 31 with poly-silicon gate electrode 34 used as a mask, whereby drain and source regions 35 and 36 are formed.

Subsequently, insulation layer 37, as shown in Fig. 1B, having a thickness of about 3,000 Å, is formed over the entire surface of substrate 31 by the CVD process in a low- or high-temperature oxidizing atmosphere. Insulating layer 37 is then formed in a portion corresponding to source region 35 with contact hole 38 by a photo-engraving process.

Contact layer 39, as shown in Fig. 1C, is them formed on the entire top surface of the semiconductor structure shown in Fig. 1B. Where conductive layer 39 is formed from a poly-silicon layer, ions are implanted into the poly-silicon layer or an impurity is diffused in it, thus reducing the resistance of the poly-silicon layer and also reducing the resistance of the junction between the poly-silicon layer 39 and drain region 35. Silicon nitride layer 40 with a thickness of about 1,000 Å, is then formed by the CVD process for instance, on conductive layer 39. Silicon nitride layer 40 is then patterned to form silicon nitride film 40a as a mask for a contact electrode. Silicon nitride layer 40 is patterned at this time such that silicon nitride film 40a from the area of contact hole 38 in drain region 35 to an area covering a portion of gate electrode 34.

The semiconductor structure thus obtained, shown in Fig. 1C, is then thermally oxidized in an atmosphere at 900 to 1,000°C, whereby poly-silicon layer 39 is oxidized except for its portion under silicon nitride film 40, as shown in Fig. 1D. As a result, poly-silicon layer 39 is divided into oxide layer 41 and conductive

layer 42. Conductive layer 42 has a portion contiguous with drain region 35 in contact hole 38, while the rest of it extends over silicon gate electrode 34. It is to be noted that oxide layer 41 and contact layer 42 are formed simultaneously such that they are self-aligned by mask 40.

Silicon nitride mask 40a of the semiconductor structure shown in Fig. 1D, is then selectively removed, according to write data. In this case, a photoresist layer is formed over silicon nitride film 40a and conductive layer 42 and then is selectively removed by the photo-engraving process using a mask corresponding to the write data. Silicon nitride film 40a over drain region 35 to be connected to data line is removed, shown in Fig. 1E, while that which is on drain region 35 not connected to data line is left. Subsequently, aluminum layer 34 is formed over the entire top surface of the semiconductor structure. Aluminum layer 43 is patterned into data lines.

Fig. 2 is a plan view showing a ROM obtained by the process shown in Figs. 1A to 1E. Fig. 3 is a section taken along line B-B' in Fig. 2. In the ROM structure shown in Figs. 2 and 3, poly-silicon layer 34 constitutes word lines, and data lines 45 are formed by patterning process of aluminum layer 43. A memory cell is shown enclosed in a dashed rectangle. In the ROM shown in Fig. 3, in the left side ROM drain region 35 is connected to data line 45 by poly-silicon layer 42. On the other hand, on the right side memory cell drain region 35 is not connected to data line 45 because of the presence of nitride layer 40a between data line 45 and poly-silicon 42.

With the ROM described above according to the invention, when electrode film 42 contiguous to drain regions is selectively connected to aluminum data line 45, nitride film 40a used to form electrode films 42 is selectively removed, and aluminum wiring for the drain

regions is done depending on the presence or absence of the nitride films 40a. For this reason, no contact holes are needed for the aluminum wiring, that is, no margin for contact holes is necessary. Integration density, thus can be improved.

Since aluminum wiring layer 45 and contact film 42 are made contiguous with one another without agency of any contact hole, fining patterning of the aluminum wiring layer will not lead to a problem of contact resistance increase due to aluminum layer grain size. Since no contact hole is formed, contact film 42 and insulating layer 41 are free from stepped portions. It is thus possible to eliminate otherwise possible disconnection of data lines at stepped portion. In addition, the thickness of the aluminum wiring layer may be reduced, so that it is possible to avoid the problem of electro-migration of aluminum.

Fig. 4 shows a different embodiment of the invention. In this instance, drain region 35 includes region 35a having the same depth as the source region and region 35b deeper than region 35a. Deeper region 35b is contiguous to field oxide layer 32. Further, unlike the embodiment of Fig. 3, poly-silicon layer 42 is doped an impurity different from the impurity contained in drain region 35, e.g., phosphorus. In this case, phosphorus introduced into poly-silicon layer 42 is re-diffused into drain region 35 in diffusion process, whereby drain region 35 is formed from deeper drain region 35b.

Figs. 5 and 6 show a further embodiment of the invention. In this instance, the entire surface of the semiconductor structure shown in Fig. 1A is thermally oxidized, whereby poly-silicon gate electrode 34 is enclosed in insulation layer 46, as shown in Fig. 7A. Then, poly-silicon layer 39 is formed on semiconductor structure 31, as shown in Fig. 7B. Then, nitride films 40a are selectively formed on poly-silicon 39 in the same manner as described before in connection with

Fig. 1C. Subsequently, processes as described before in connection with Figs. 1D and 1E are performed to obtain the ROM.

Fig. 8 shows a further embodiment. In this instance, poly-silicon contact film 42 under nitride film 40a does not extend up to the region of gate electrode 34, but is substantially confined in contact hole 38 provided on drain region 35. Even with this structure, a sufficient area of contact between data line 45 and contact film 42 can be obtained.

In the embodiments described above, the gate electrode of the MOS transistor functioning as memory cell, i.e., the word line, is constituted by poly-silicon. However, it is also possible to form word lines having a double-layer structure formed of a high-melting metal, e.g., molybdenum silicide, and poly-silicon. Generally, the layer may be made of a conductive material which can contain impurities.

Further, the above embodiments have concerned with the N-channel ROMs using a p-type semiconductor substrate. However, this is by no means limitative, and the invention is applicable to either an n-well C MOS structure ROM using a p-type semiconductor substrate or to a C MOS structure ROM where a p-well is formed in an n-type semiconductor substrate.

Claims:

1. A semiconductor read only memory device comprising:

a plurality of memory cells each including a pair of semiconductor regions separately formed on a semiconductor substrate of a first conductivity type, said semiconductor regions having a second conductivity type opposite to said first conductivity type, and a gate electrode insulatively disposed over said semiconductor substrate and extending between said pair of semiconductor regions;

characterized in that

a first conductive layer (39) is contiguous to one of said semiconductor regions of each of said memory cells and contains an impurity of said second conductivity type;

a mask layer (40a) is formed selectively on said first conductive layer (39) according to write information and having electric insulation property and anti-oxidation property; and

a second conductive layer (43) is formed on the surface of said first conductive layer inclusive of said mask layer and selectively contiguous to said first conductive layer depending on the presence or absence of said mask layer.

2. The semiconductor read only memory device according to claim 1, characterized in that said first conductive layer (39) is made of a poly-silicon layer.

3. The semiconductor read only memory device according to claim 1, characterized in that said mask layer (40a) is made of silicon nitride.

4. A method of manufacturing a semiconductor read only memory device comprising:

a step of forming a field oxide layer (32) selectively on a semiconductor substrate (31) of a first conductivity type to obtain a plurality of separated

semiconductor sections for forming respective memory cells therein;

a step of forming an insulated gate electrode (34) on each of said separated semiconductor sections of said semiconductor substrate;

a step of doping said semiconductor substrate with an impurity of said second conductivity type with each said field oxide layer (32) and said insulated gate electrode (34) used as a mask to thereby form first and second semiconductor regions (35, 36) of said second conductivity type separated from each other in each of said separated semiconductor sections;

characterized by including:

a step of insulatively disposing over said semiconductor substrate a first conductive layer (39) contiguous to each of said first semiconductor regions (35) and containing an impurity of said second conductivity type;

a step of forming an anti-oxidation layer (40) over the entire surface of said first conductive layer (39);

a step of selectively removing said anti-oxidation layer to leave a portion corresponding to each said first semiconductor region contiguous to said first conductive layer, thus forming anti-oxidation masks (40a);

a step of selectively oxidizing using said anti-oxidation masks, portions of said first conductive layer (39) other than portions corresponding to said first semiconductor regions;

a step of selectively removing said anti-oxidation masks (40a) according to write data;

a step of forming a second conductive layer (43) on the entire surface of said anti-oxidation layers and said first conductive layer; and

patterning said second conductive layer (43) to form a wiring layer contiguous to said electrode films or insulated from the same by said anti-oxidation masks.

5. The method according to claim 4, characterized in that said step of forming said first conductive layer

includes a step of forming an insulation layer (37) over the entire surface of said semiconductor substrate (31) inclusive of said insulated gate electrodes, a step of forming contact holes (38) selectively in said insulation layer, and a step of forming said first conductive layer on the entire surface of said insulation layer such that said first conductive layer is in contact with said first semiconductor regions in said contact holes.

6. A method according to claim 4, characterized in that said step of forming said first conductive layer includes a step of forming an insulation layer (46) enclosing each said insulated gate electrode, and a step of forming said first conductive layer on the entire surface of said semiconductor substrate (31) inclusive of said gate electrodes (34) enclosed in said insulation layers.

7. The method according to claim 4, characterized in that said method of forming said anti-oxidation masks is a step of forming anti-oxidation masks each having a mask film (40a) extending from the area of each said first semiconductor region to the area of a portion of each said gate electrode.

8. The method according to claim 4, characterized in that said step of forming said anti-oxidation masks is a step of forming anti-oxidation layers each having a mask film (40) substantially confined in the area of each said first semiconductor region.

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FIG. 1A

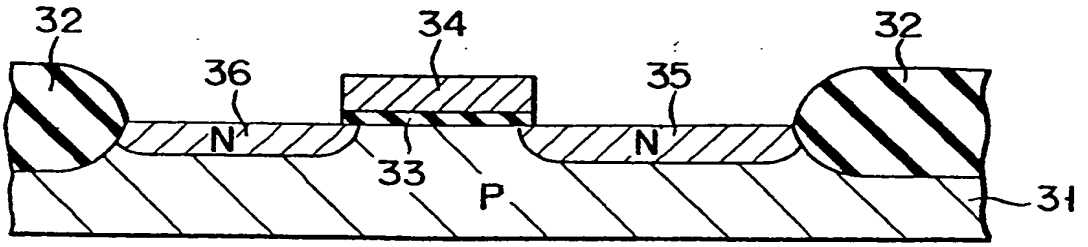

FIG. 1B

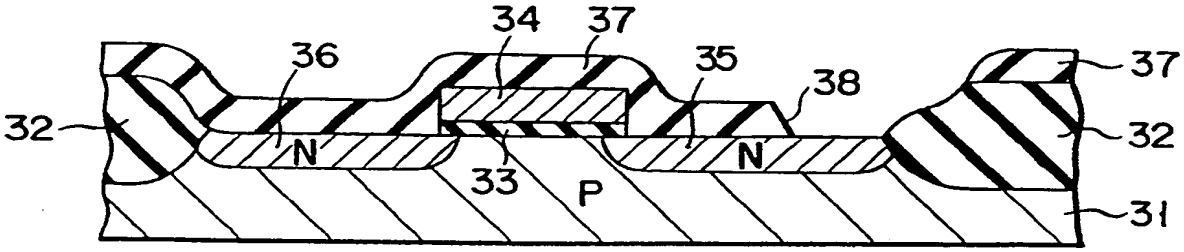

FIG. 1C

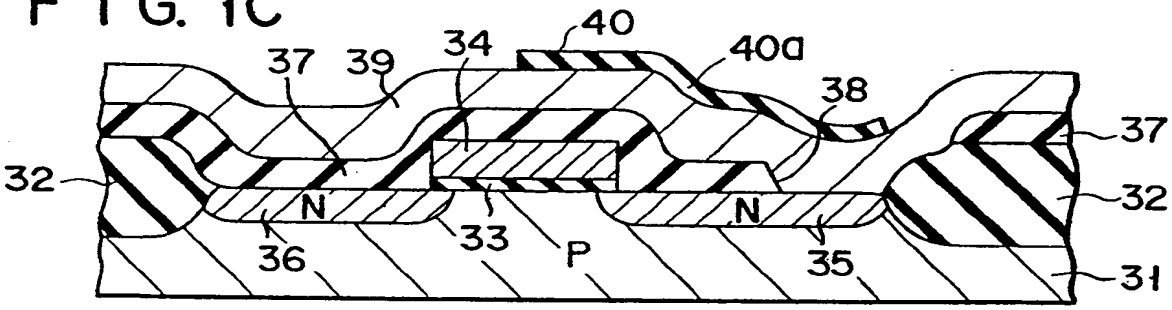

FIG. 1D

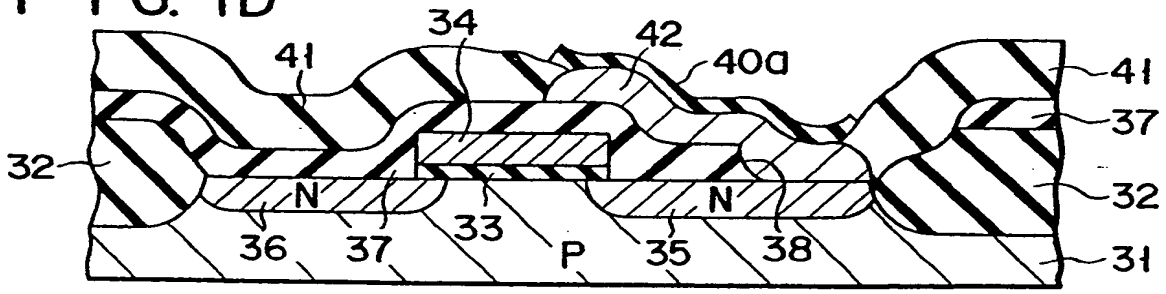

FIG. 1E

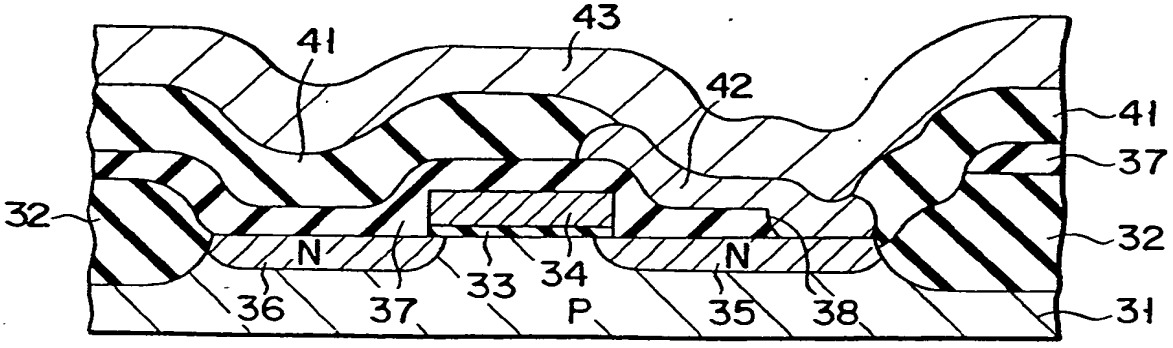

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FIG. 2

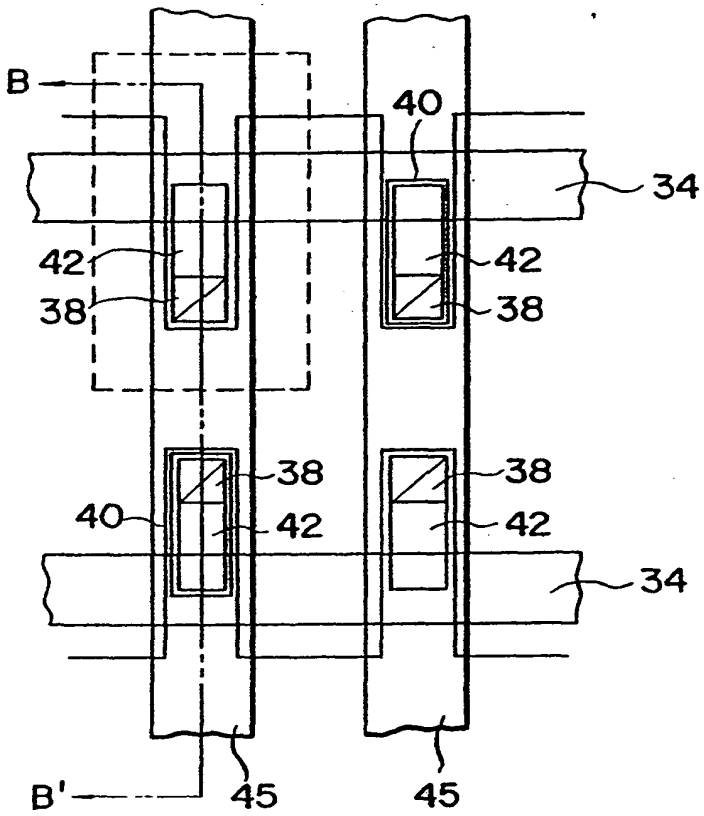

FIG. 3

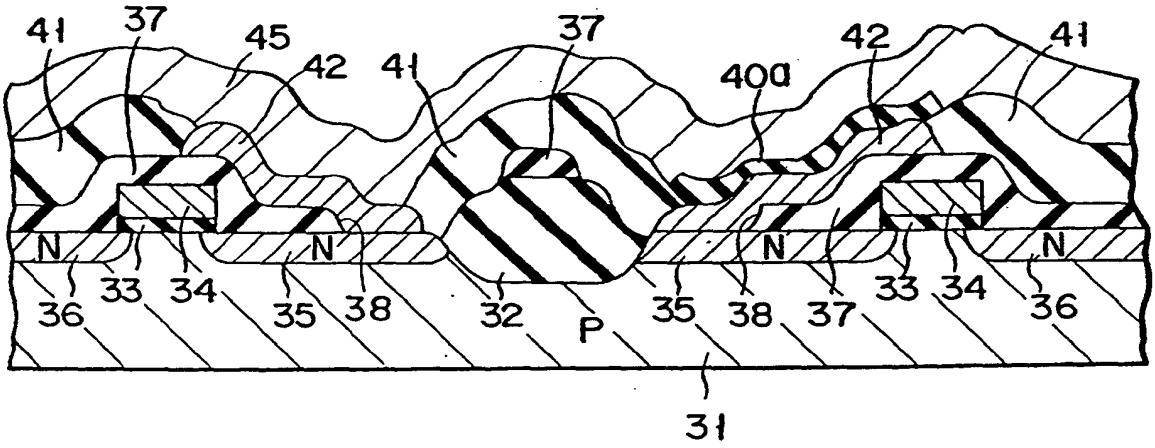

FIG. 4

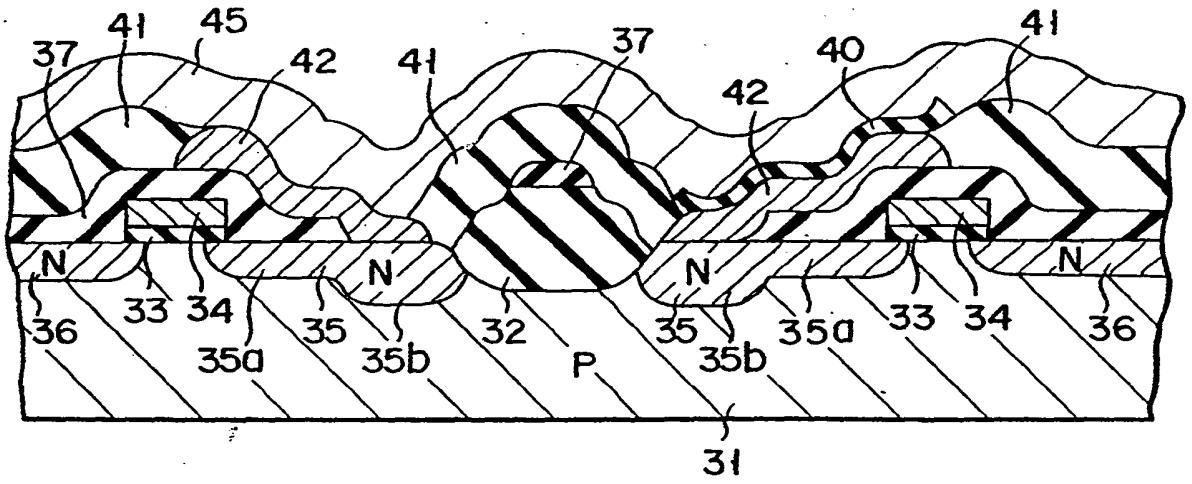

FIG. 5

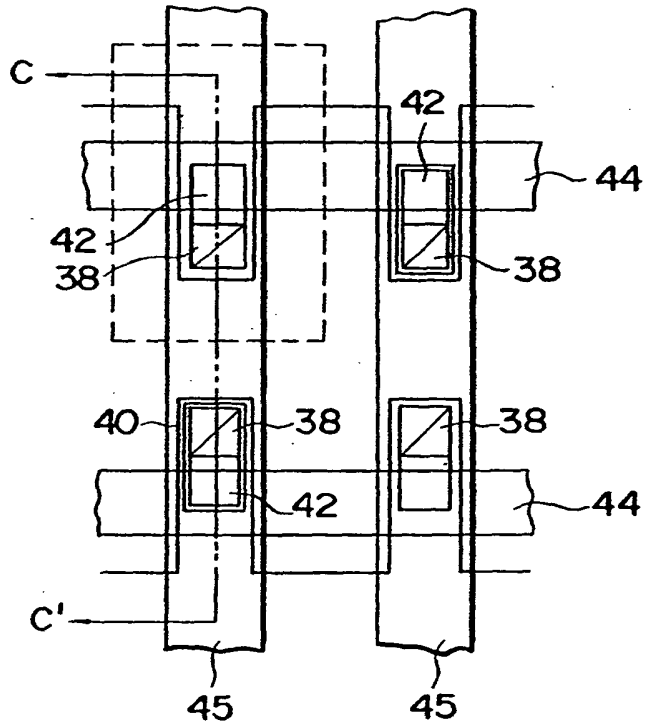

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FIG. 6

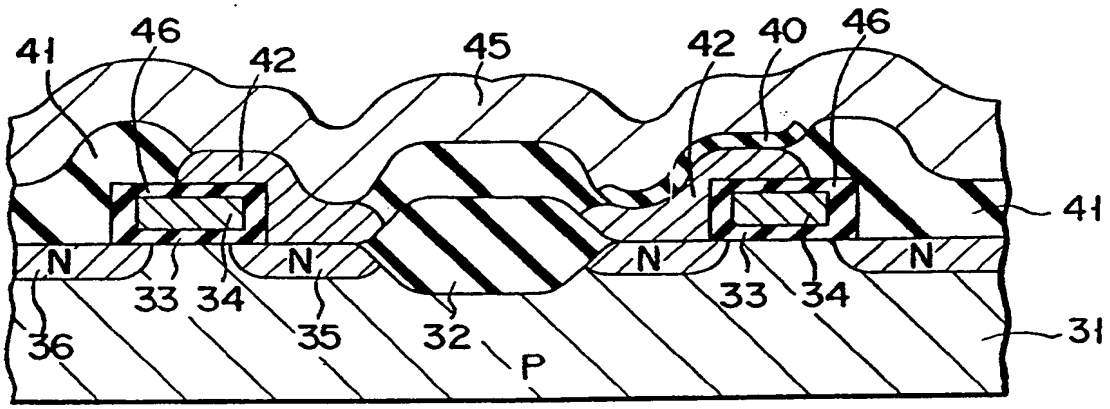

FIG. 8

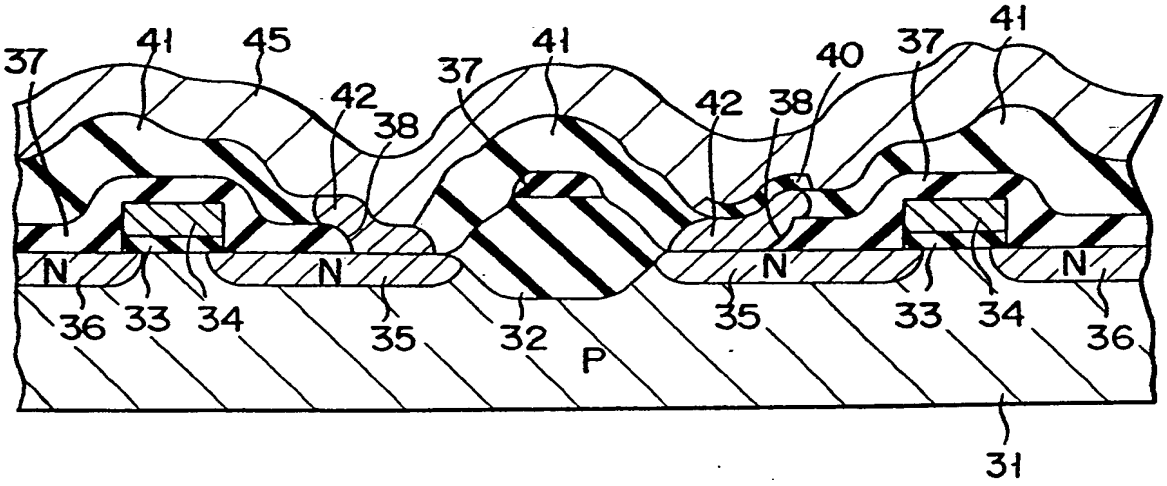

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FIG. 7A

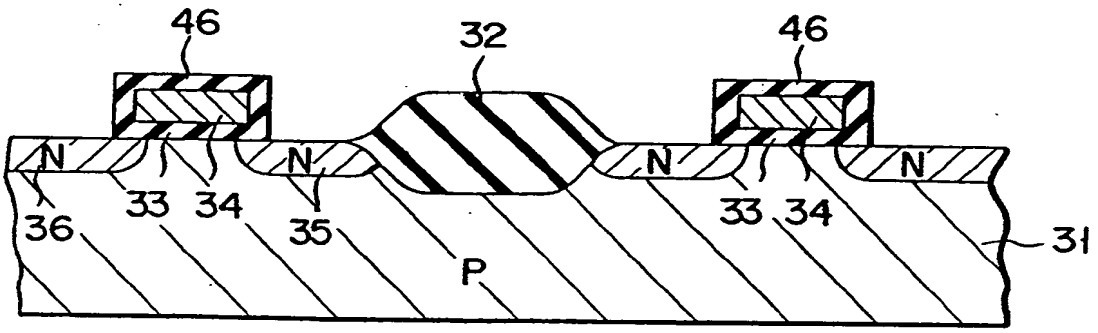

FIG. 7B

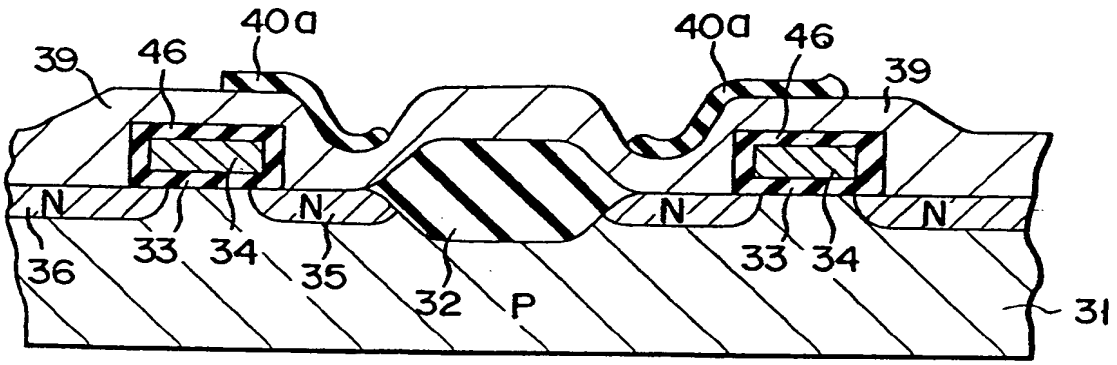

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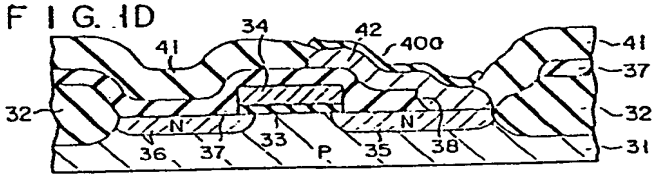
FIG. 1D



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European Patent Office

EUROPEAN SEARCH REPORT

0186855
Application number

EP 85 11 6126

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
A	EP-A-0 124 115 (TOSHIBA) * Claims 1,2,4 *	1,2,4, 5	H 01 L 27/10 G 11 C 17/00
A	EP-A-0 054 102 (ROCKWELL) * Page 8, lines 21-29; page 9, lines 5-26; page 10, lines 1-22 *	4	
A	INTERNATIONAL ELECTRON DEVICES MEETING, TECHNICAL DIGEST, Washington, D.C., US, 3rd-5th December 1979, pages 585-588, IEEE, New York, US; H. GOTO et al.: "A new self-aligned source/drain diffusion technology from selectively oxidized poly-silicon" * Figure 5; left-hand column, paragraph 2 *	3,4	
A	EP-A-0 036 573 (IBM) * Figures 2-7; page 6, lines 6-25 *	6	TECHNICAL FIELDS SEARCHED (Int. Cl.4) H 01 L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	17-07-1986	MACHEK, J.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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